PRODUCT SPECIFICATION

Part No.:	**AC-OP-8G800-01**	
Description:	800G OSFP SR8 , MMF 850nm 100m	
Release Date	**Rev.**	**Revision Change Description**
2024/04/30	A0	New Release
2024/09/08	A1	Update the Mechanical drawing
2025/09/03	A2	Version Update

Features

- Data Rate 106.25 Gb/s PAM4 per lane
- Digital Diagnostics Monitoring Interface
- Reach up to 100m over MMF(OM4)
- Hot-pluggable OSFP form factor
- 850nm VCSEL laser and PIN receiver
- Commercial operating case temperature range: 0~ 70ºC
- MPO-16 APC or 2xMPO-12 APC connector
- RoHS-6 compliant
- TDEC< 4.4dB
- Single 3.3V power supply
- Power dissipation< 14W

Application

- Data center
- 800G-SR8

Standard

- IEEE Std 802.3ck
- 800G OSFP MSA and CMIS 5.1

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Specification:

Absolute Maximum Ratings				
Parameter	**Symbol**	**Min**	**Max**	**Unit**
Storage Ambient Temperature	T_{STG}	-40	85	℃
Operating Humidity	H_O	5	85	%
Power Supply Voltage	Vcc	-0.3	3.6	V
Signal Input Voltage		Vcc-0.3	Vcc +0.3	V

Recommended Operating Conditions					
Parameter	**Symbol**	**Min**	**Typical**	**Max**	**Unit**
Operating Case Temperature	Tc	0		70	℃
Power Supply Voltage	Vcc	3.13	3.3	3.47	V
Data Rate, each Lane（PAM4）			106.25		Gbps
Fiber Length 50/125μm core MMF		-	-	100	m

Optical transmitter Characteristics						
Parameter	**Symbol**	**Min**	**Typical**	**Max**	**Unit**	**Notes**
Launched Power (avg.) Per Lane	Pavg	-4.6		4	dBm	
Wavelength Range	λ0	844	850	863	nm	
Spectral Width(-20dB)	Δλ			0.6	nm	
Extinction Ratio	ER	2.5			dB	
Transmitter OFF Output Power	POff			-30	dBm	
Optical Modulation Amplitude(OMA outer)	OMA	-2.6		3.5	dBm	
Transmitter and dispersion eye closure(TDECQ)	TDECQ			4.4	dB	

Optical receiver Characteristics						
Parameter	**Symbol**	**Min**	**Typical**	**Max**	**Unit**	**Notes**
Receiver Wavelength Range		844	850	863	nm	
Average Receiver Power Per Lane		-6.4		4	dBm	
Receiver Sensitivity（OMAouter） Max(TECQ, TDECQ) ≤1.8dB 1.8<max(TECQ, TDECQ) ≤	PSen			-4.6 -6.4+TECQ	dBm	1

4.4dB						
Optical Power Input Overload	P_{in-max}	3.5			dBm	
Receiver Reflectance	Rr			-12	dB	

Notes:

1. BER=2.4E-4; PRBS31Q@53.125GBd.

Pin Definition

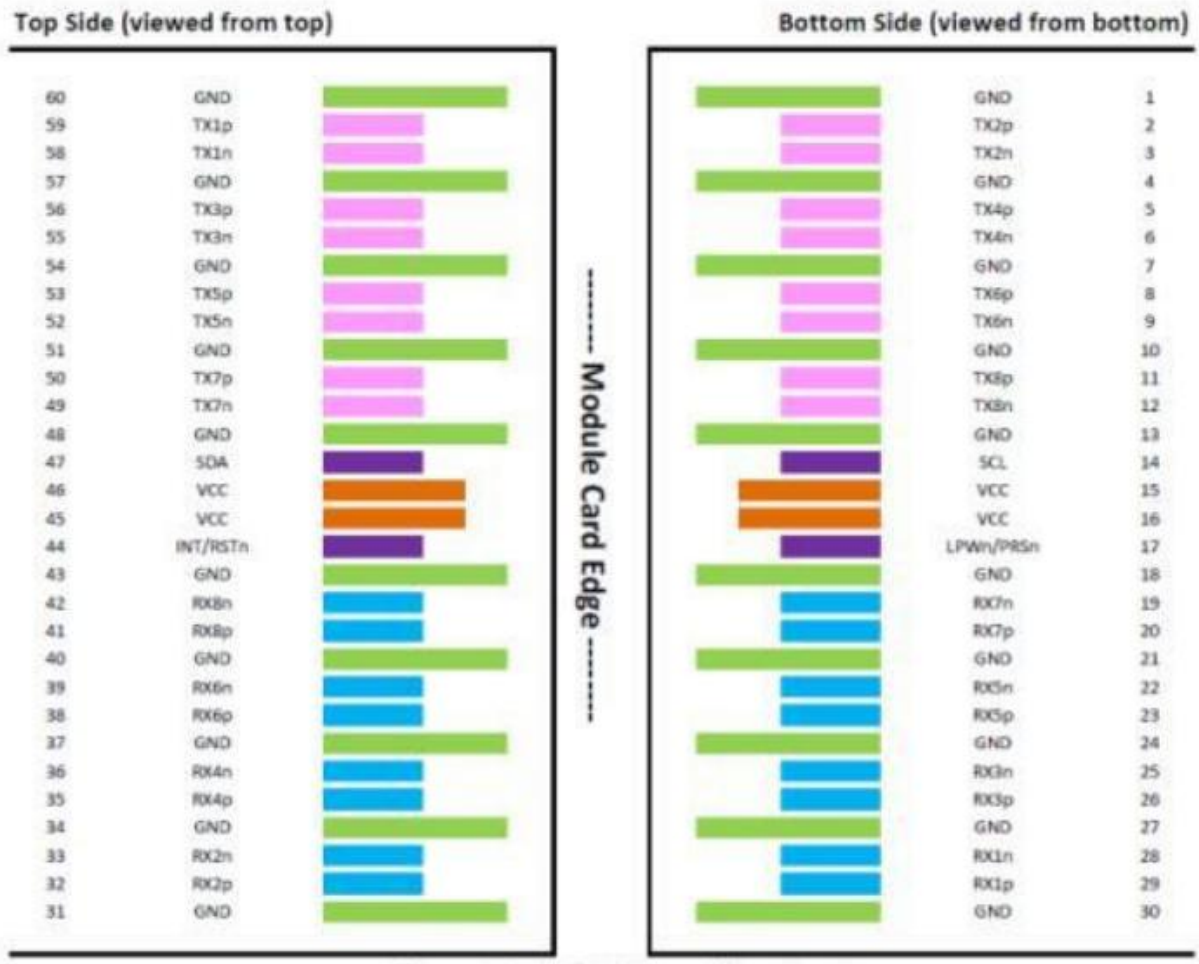


Figure1 OSFP 60-pin connector

Pin	Symbol	Description	Logic	Direction	Plug Sequence	Note
1	GND	Ground			1	
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3	
4	GND	Ground			1	
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3	
7	GND	Ground			1	
8	TX6p	Underfined	CML-I	Input from Host	3	
9	TX6n	Underfined	CML-I	Input from Host	3	
10	GND	Ground			1	
11	TX8p	Underfined	CML-I	Input from Host	3	
12	TX8n	Underfined	CML-I	Input from Host	3	
13	GND	Ground			1	

14	SCL	2-wire Serial interface clock	LVCMOS- I/O	Bi-directional	3	Open-Drain with pull up resistor on H
15	VCC	+3.3V Power		Power from Host	2	
16	VCC	+3.3V Power		Power from Host	2	
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3	See pin description for required circuit
18	GND	Ground			1	
19	RX7n	Underfined	CML-O	Output to Host	3	
20	RX7p	Underfined	CML-O	Output to Host	3	
21	GND	Ground			1	
22	RX5n	Underfined	CML-O	Output to Host	3	
23	RX5p	Underfined	CML-O	Output to	3	
24	GND	Ground			1	
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3	
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
27	GND	Ground			1	
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3	
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
30	GND	Ground			1	
31	GND	Ground			1	
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3	
34	GND	Ground			1	
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3	
37	GND	Ground			1	
38	RX6p	Underfined	CML-O	Output to Host	3	
39	RX6n	Underfined	CML-O	Output to Host	3	
40	GND	Ground			1	
41	RX8p	Underfined	CML-O	Output to Host	3	
42	RX8n	Underfined	CML-O	Output to Host	3	
43	GND	Ground			1	
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3	See pin description for required circuit
45	VCC	+3.3V Power		Power from Host	2	
46	VCC	+3.3V Power		Power from Host	2	
47	SDA	2-wire Serial interface data	LVCMOS- I/O	Bi-directional	3	Open-Drain with pull up resistor on Host
48	GND	Ground			1	
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3	

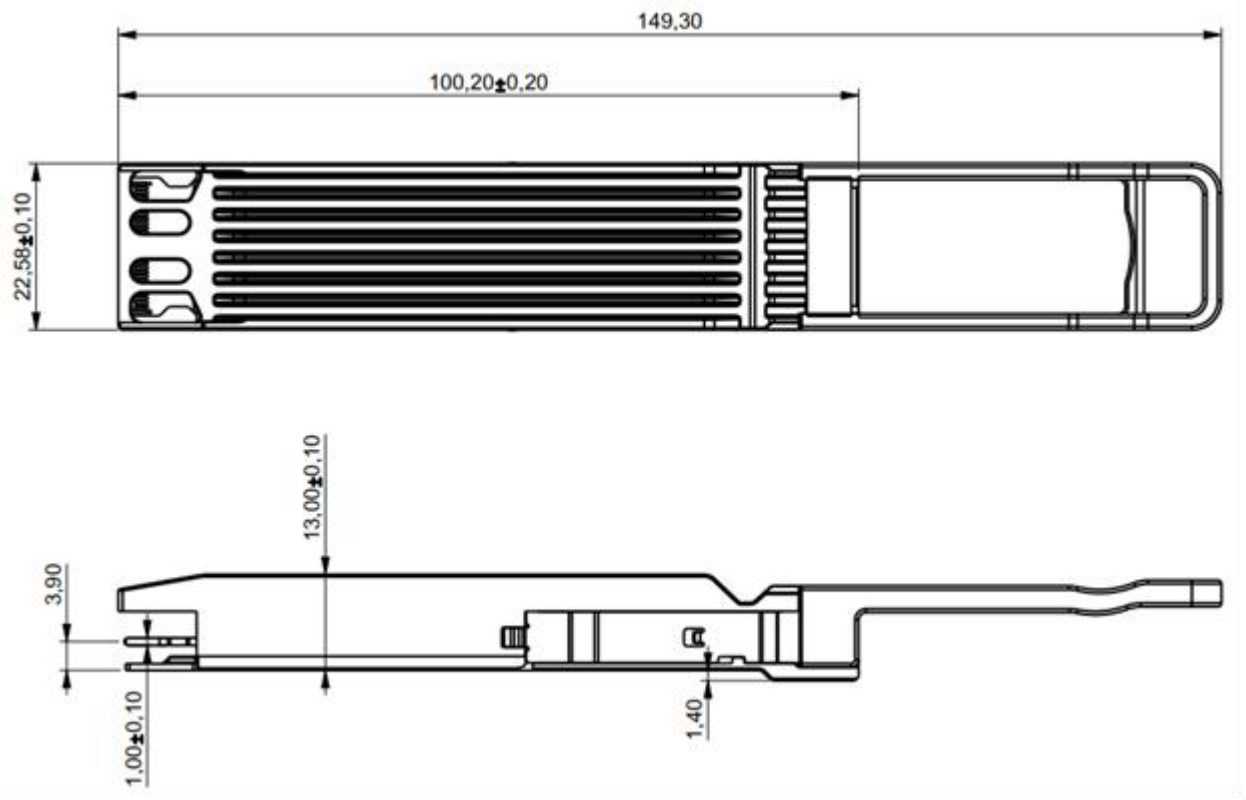
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
51	GND	Ground			1	
52	TX5n	Underfined	CML-I	Input from Host	3	
53	TX5p	Underfined	CML-I	Input from Host	3	
54	GND	Ground			1	
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3	
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
57	GND	Ground			1	
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3	
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
60	GND	Ground			1	

Electrical Power Supply Characteristics

Parameter	Symbol	Min	Typ.	Max	Units
Power Supply Voltage	VCC1 , VCCTx, VCCRx	3.13	3.30	3.47	V
Power Consumption	PW	-	-	10	W
Power Consumption-LP mode	-	-	-	1.5	W

Notes:The specified characteristics are met within the recommended range of operation. Unless otherwise noted typical data are quoted at nominal voltage and +25°C ambient temperature.

Package Outline



Dimensions are in millimeters. All dimensions are ±0.2mm unless otherwise specified. (Unit: mm)

Regulatory Compliance

Feature	Test	Method
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883E Method 3015.7	Class 1(>1000V for SFI pins, >2000Vfor other pins.)
Electrostatic Discharge (ESD) Immunity	IEC61000-4-2	Class 2(>4.0kV)
Electromagnetic Interference (EMI)	CISPR22 ITE Class B FCC Class B CENELEC EN55022 VCCI Class 1	Comply with standard
Immunity	IEC61000-4-3	Comply with standard
Eye Safety	FDA 21CFR 1040.10 and 1040.11 EN (IEC) 60825-1,2	Compatible with Class I laser Product

Ordering Information

Part. No	Specifications								
	Pack	Rate (Gbps)	Tx (nm)	Po (dBm)	RX	Sen (dBm)	Temp (℃)	Reach (M)	DDM
AC-OP-8G800-01	OSFP	800G	VCSEL 850	-4.6~4	PIN	<-6.4	0~70	100	Y